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Design of Low Power & High Speed Comparator with 0.18μm Technology for ADC Application

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Abstract
In Analog to Digital Converter (ADC), high speed comparator influences the overall performance of ADC directly. This paper presents the high speed & low power design of a CMOS comparator. Schematic design of this comparator is fabricated in a 0.18μm UMC Technology with 1.8V power supply and simulated in cadence Virtuoso. Simulation results are presented and it shows that this design can work under high speed of 0.8108 GHz. The design has a low offset voltage, low power dissipation 108.0318μw. In addition we have verified present results with schematic view design and also compared these results with earlier reported work and got improvement in this reported work.
Index Terms – Preamplifier based Comparator, dynamic comparator, dynamic comparator with positive feedback, Dynamic comparator with positive feedback PMOS as switch, low power, low offset, high speed, low noise, A/D Converter.

I. INTRODUCTION

The fast growing electronics industry is pushing towards high speed low power analog to digital converters. Comparator is electronic devices which are mainly used in Analog to Digital converter (ADC). In ADC they are used for quantization process, and are mainly responsible for the delay produced and power consumed by an ADC. A high speed low power comparator is required to satisfy the future demands The Comparators are used in analog-to-digital converters (ADCs), data transmission applications, switching power regulators and many other applications. The voltages that appear at the inputs are compared by the comparator that produces a binary output which represents a difference between them. They are critical components in analog-to-digital converters. Designing high-speed comparators becomes more challenging when working with smaller supply voltages. In other words, for a given technology, to attain high speed, transistors with increased width and length values are required to compensate for the reduction of supply voltage, which also means increased chip area and power. So, Transistor width and length are adjusted accordingly.

For minimum power consumption and maximum operating speed. A model for the comparator is developed and discussed, and its functionality is verified by showing a comparison of result obtained for the proposed model and the existing model. The platform used to develop and analyze the existing model Cadence Environment (Virtuoso). The comparator is basically excluded from application to the high speed A/D converters with high resolution owning to its large offset voltage which significantly affects the resolution. As a consequence, the preamplifier based comparator topology in which an amplifier is added before a latched comparator, aiming at achieving small offset voltage and high speed, has been developed . The preamplifier based comparator , which combine of an amplifier and a latch comparator can obtain high speed and low power dissipation. Thus, by considering factors of speed and power dissipation, preamplifier latch comparator is the choice of A/D converters . Block representation of the proposed design of the comparator is shown in Fig. 1. This designed comparator consists of three stages namely input stage, decision stage and output stage. The input stage (pre amplification) amplifies the input signal to improve the comparator sensitivity and isolate the input of the Comparator from switching noise coming from positive feedback stage . The decision circuit is the heart of the comparator and should be capable of discriminating mV level signals and it is used to determine which of the input signals is larger .The final stage is the output stage (post amplification) . The final component in our comparator design is the output buffer or post-amplifier. The main purpose of the output buffer is to convert the output of the decision circuit into a logic signal (i.e., 0 or 5V).
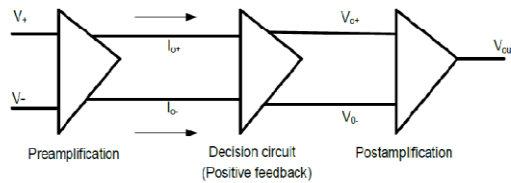
Figure 1. Block diagram of preamplifier based comparator

II. DESIGN SPECIFICATION

A. Clock frequency

The clock frequency *"fc"* is defined as the reciprocal of the time interval *T*, as:

$$f_c = 1/T \tag{1}$$

The clock frequency has to be equal or greater than twice of the frequency bandwidth of analog signals .

B. Power dissipation

The power dissipated by comparator is simply the product of the sum of the current flowing in the current source with power supply voltage. We were primarily considering high speed and low voltage. Dynamic comparator power dissipation resembles that of digital gates, which have a power dissipation given approximately by :

$$p = fcv_{DD}^{2} \tag{2}$$

Where,

f = output frequency,

V_{DD} = supply voltage

C = output capacitance

If a square pulse is applied to the input of the comparator with a period t and frequency *f,* the average amount of current that the comparator must pull from V_{DD}, recalling the current is being supplied from V_{DD} only when p-channel is on. Notice that the power dissipation is a function of the clock frequency. A great deal of effort is put into reducing the power dissipation in CMOS circuits. One of the major advantages of dynamic logic is its power dissipation.

C. Offset Voltage

The offset of this stage is dependent on both the input amplifiers and the latching stage. Input-offset voltage can be a particularly difficult problem in comparator design. In precision applications, such as high-resolution converters, large input-offset voltages cannot be tolerated. The offset-voltage of the comparator is reduced, using either Input Offset Storage (IOS) or Output Offset Storage (OOS) around the comparator preamplifier. In the IOS configuration, the preamplifier must be stable in the unity feedback configuration. Also, the MOSFETs of the preamplifier must remain in saturation when the offset voltage is stored on the capacitors. For the IOS scheme the input storage capacitance must be much

larger than the input capacitance of the preamplifier, so that the storage capacitors do not attenuate the input signals. For the OOS scheme the storage capacitors should be much larger than the input capacitance of the dynamic latch. The total offset voltage of the comparator consists of the sum of both source coupled pairs. The offset of one differential pair has the well-known dependency on the mismatch of the threshold voltage ΔV_T, load resistance ΔR_L and transistor dimensions $\Delta\beta$ and their corresponding average values V_T, R_L, and β.

$$V_{OS} = \Delta V_T + \frac{V_{gs} - V_T}{2}\left(\frac{\Delta R_L}{R_L} + \frac{\Delta\beta}{\beta}\right) \tag{3}$$

III. DESIGN OF COMPARATORS

Fig.5 presents the schematic view of the proposed design. In this when clock (Clk) is low, the latch comparator is reset, and at this time Clk1 is high, latch-comparator can receive the amplified signal of preamplifier. Fig.2 is a schematic diagram differential amplifier which amplifies the input signal which enhances the sensitivity of comparator. Fig.3 is schematic diagram of latch circuit also known as heart of the comparator . Fig.4 is schematic diagram of output buffer, this part of comparator is needed to amplify the signal coming from latch and to provide enough current for the load
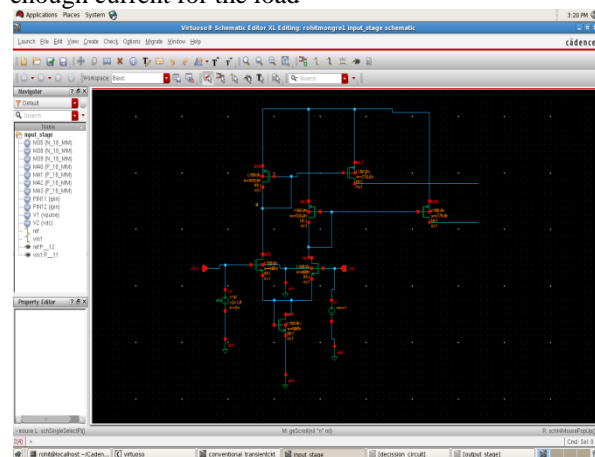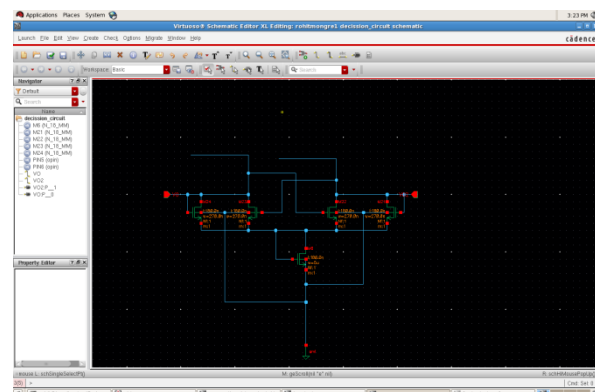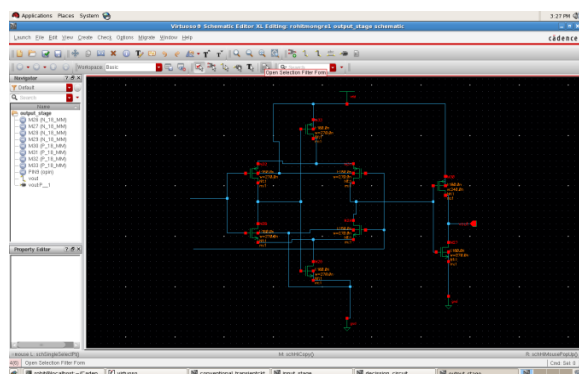

Fig :2

Fig:3

Fig:4 output stage (post amplification).

Preamplification

This circuit is a differential amplifier with active loads. The sizes of NM0 and NM1 are set by considering the diff-amp transconductance and the input resistance. The transconductance sets the gain of the stage, while the input capacitance of the comparator is determined by the size of NM0 and NM1. We will concentrate on speed in the design, and therefore we will set the channel lengths of the MOSFETs to 180nm. (Channel length modulation gives rise to an unwanted offset voltage). Using the sizes given in the schematic, we can relate the input voltages to output currents by

$$i_{o+} = \frac{gm}{2}(v_+ - v_-) + \frac{Iss}{2} = Iss - i_{o-} \ .$$

$$g_m = g_{m1} = g_{m2}$$

To further increase the gain of the first stage, we can size up the widths of MOSFETs PM3 and PM4 relative to the widths of PM0 and PM1.

Decision circuit

The decision circuit is the heart of the comparator and should be capable of discriminating mV level signals. We should also be able to design the circuit with some hysteresis for use in rejecting noise on a signal. The circuit uses positive feedback from the cross-gate connection of NM1 and NM2 to increase the gain of the decision element. Let's begin by assuming that $io+$ is much larger than $io-$ so that M5 and M7 are ON and NM1 and NM3 are off. We will also assume that $\beta NM0 = \beta NM3 = \beta A$ and $\beta NM1 = \beta NM2 = \beta B$. Under these circumstances, vo- is approximately 0V and vo+ is

If we start to increase $io-$ and decrease $io+$, switching takes place when the drain-source voltage of NM2 is equal to VTHN of NM1. At this point, NM1 starts to take current away from NM0. This decreases the drain-source voltage of NM0 and thus starts to turn NM2 off. If we assume that the maximum value of vo+ or vo- is equal to 2VTHN

,then NM1 and NM2 operate, under steady state $\beta A = \beta 5 = \beta 8$, $\beta B = \beta 6 = \beta 7$.
Conditions, in either cutoff or the triode regions. Under these circumstances, the voltage across NM2 reaches VTHN, and thus NM2 enters the saturation region, when the current through NM2 is

$$i_{o-} = \frac{\beta B}{2}(v_{o+} - V_{THN})^2 = \frac{\beta B}{\beta A} \cdot i_{o+}$$

This is the point at which switching takes place. That is , NM2 shuts off and NM1 turns on. If $\beta A = \beta B$, then switching takes place when the currents $io+$ and $io-$ are equal. Unequal βs cause the comparator to exhibit hysteresis. A similar analysis for increasing $io+$ and decreasing $io-$ yields a switching point of

$$i_{o+} = \frac{\beta B}{\beta A} \cdot i_{o-}$$

$$v_{o+} = \sqrt{\frac{2io+}{\beta A}} + V_{THN}$$

Output Buffer:-

The final component in our comparator design is the output buffer or post-amplifier. The main purpose of the output buffer is to convert the output of the decision circuit into a logic signal (i.e., 0 or 5V). The output buffer should accept a differential input signal and not have slew-rate limitations. The circuit used as an output buffer in our basic comparator design .This circuit is a self-biasing differential amplifier. We can see a problem in connecting the decision circuit directly to the output buffer. The MOSFET NM3 is added in series with the decision circuit to increase the average voltage out of the decision circuit. The size of the MOSFET is somewhat arbitrary. We will set W17/L17 =5 μm/100nm so that the output of the decision circuit is increased by approximately VTHN

Design I : Proposed Comparator
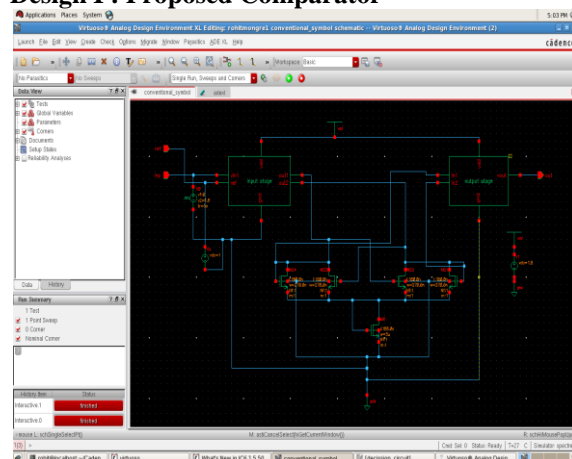
The complete schematic of the comparator is shown in fig . Here the input Voltage as a ref parameter. And sweep this parameter from 0 to 1.8 V. The reference Voltage as 1 Volt. So as above the Circuit is connected and the wave forms of the Output Voltages of Decision Circuit and Output Buffer are shown in Fig . Here the reference Voltage as 1V.So if the input Voltage is greater than reference Voltage it is giving output Voltage as logic 1.And if the Input Voltage is less than reference Voltage it gives the Output as logic 0.And also the output waveforms are shown. These waveforms are also changing at the reference Voltage.

Transient analysis

    To calculate the delay of the comparator Transient analysis is needed. Here I have given input pulse to the one input of the Pre-amplifier. And I have given 500mv DC Voltage to the other end of the Pre-amplifier.

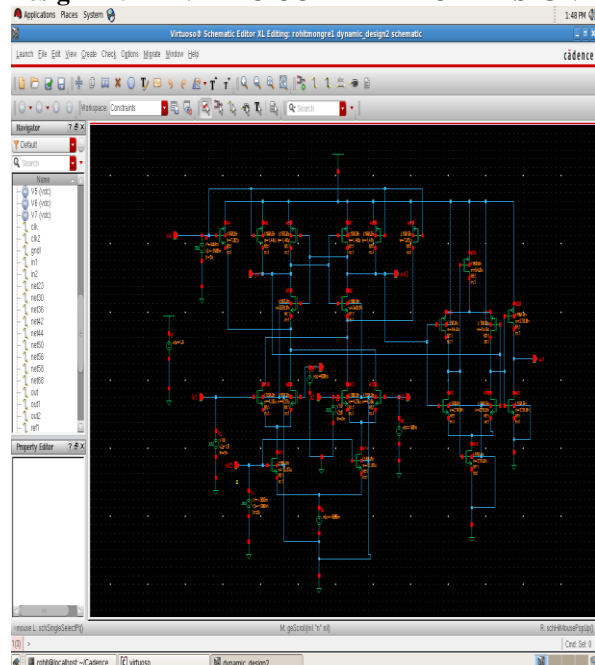Fig:6 Transient Analysis of Preamplifier based Comparator
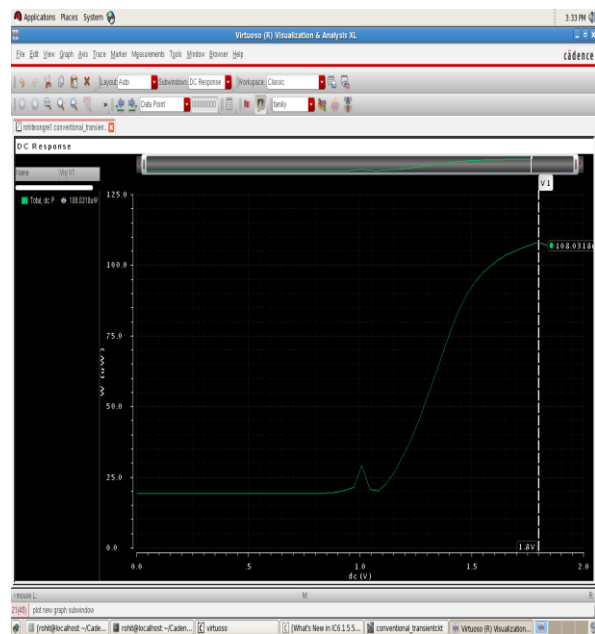
Fig:7 Power Dissipation of Preamplifier based Comparator
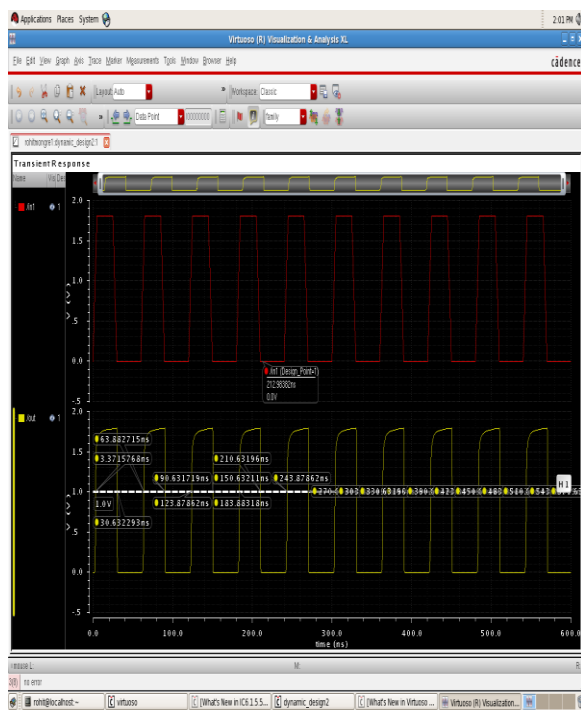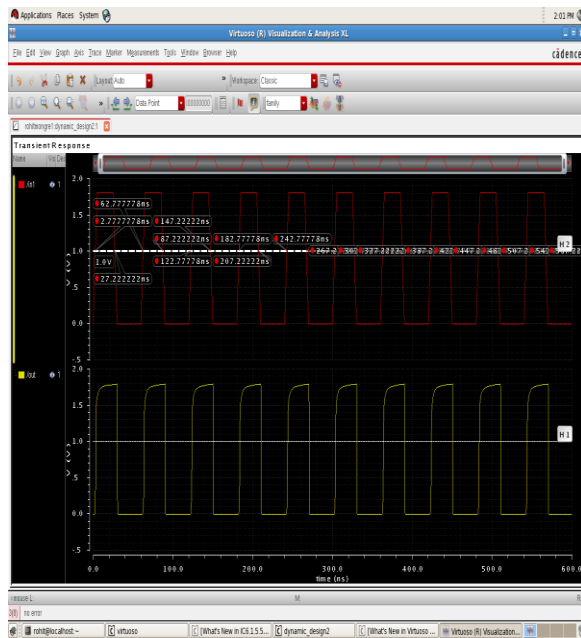
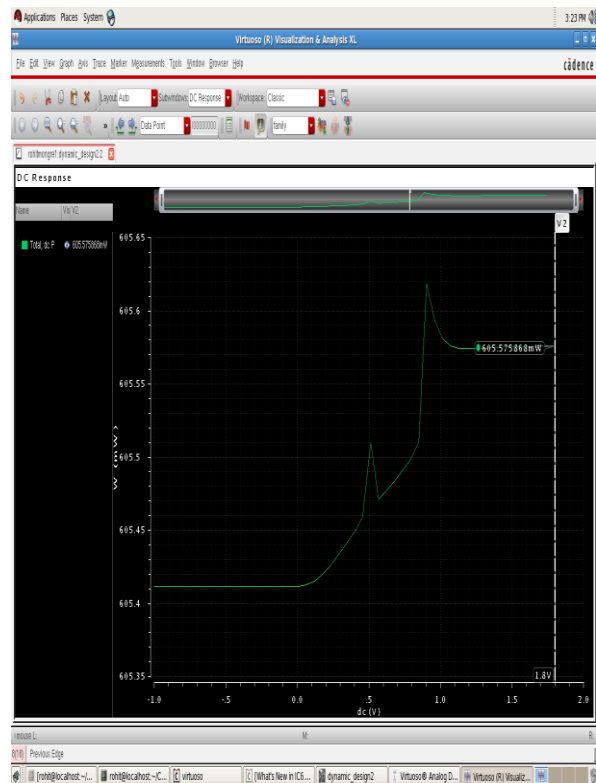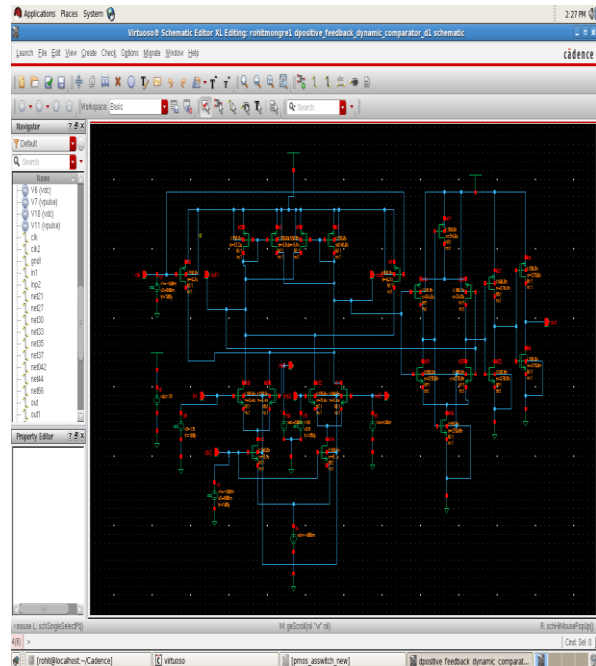**Design II : DYNAMIC COMPARATOR DESIGN**

Fig:10 Power Dissipation of Dynamic Comparator

Design III: Dynamic comparator with positive feedback

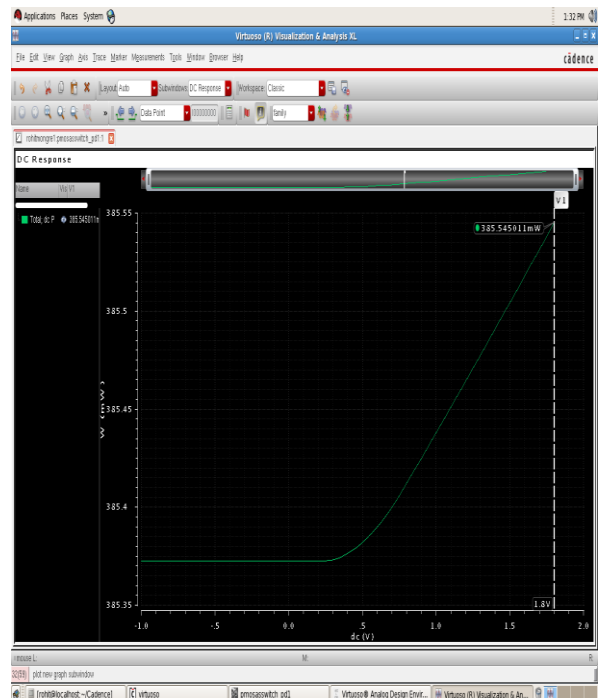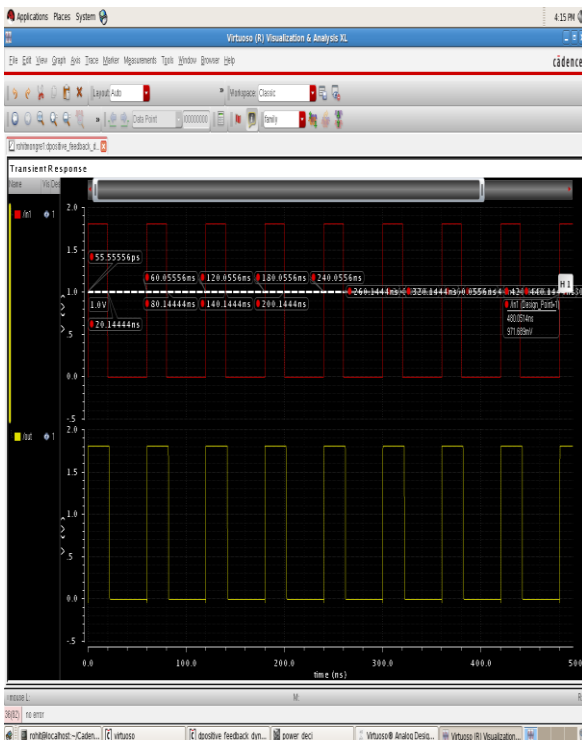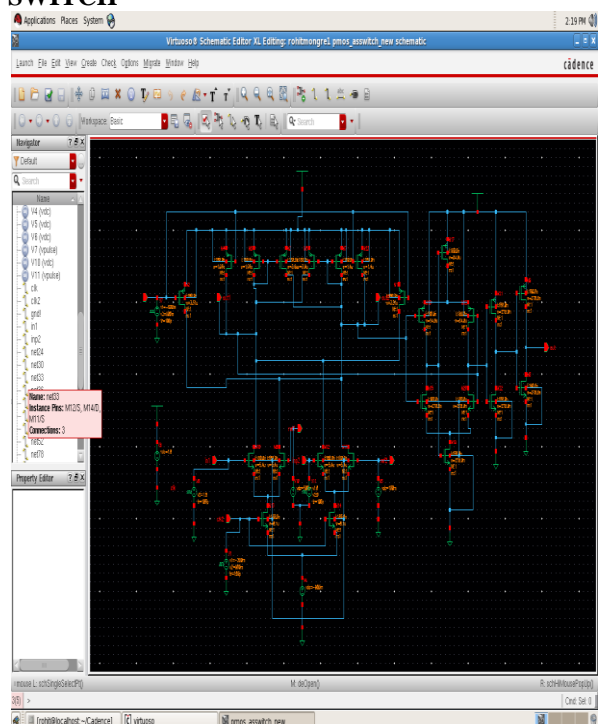**Fig : 9 Transient Analysis of Dynamic Comparator.**

Fig:13 Power Dissipation of Dynamic comparator with positive feedback.

Design IV: DYNAMIC COMPARATOR USING POSITIVE FEEDBACK USING PMOS AS A SWITCH
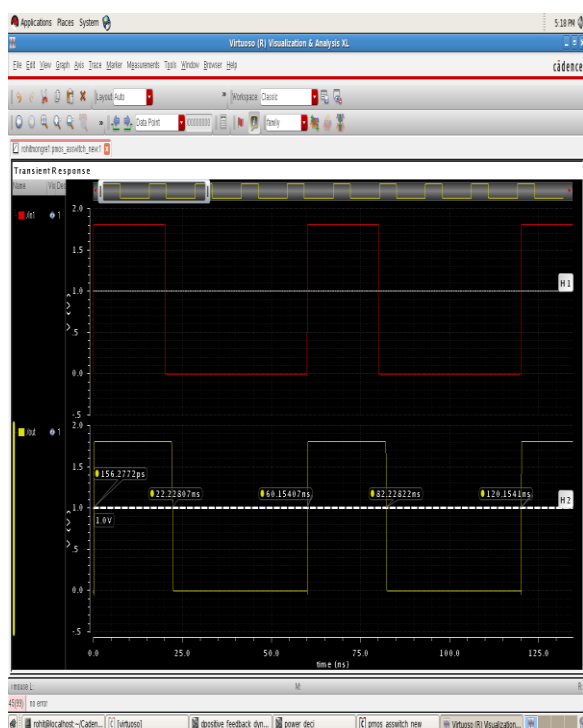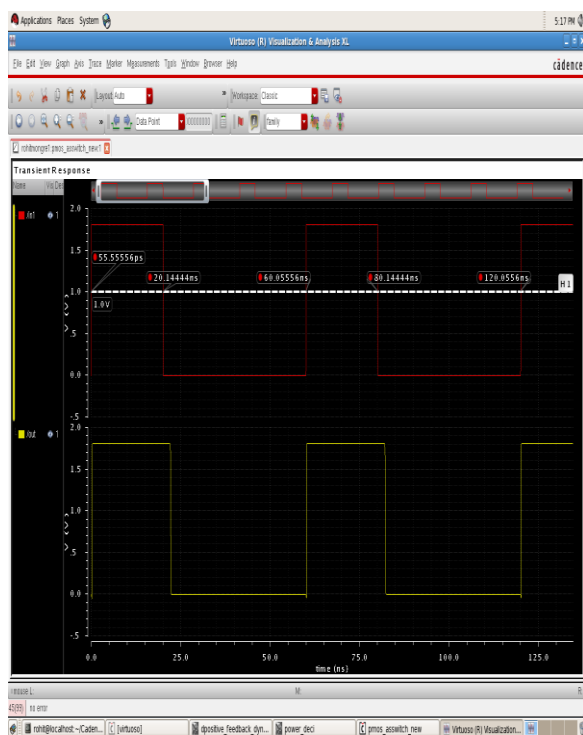
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Fig:16 Power Dissipation of Dynamic Comparator with positive feedback using PMOS as Switch

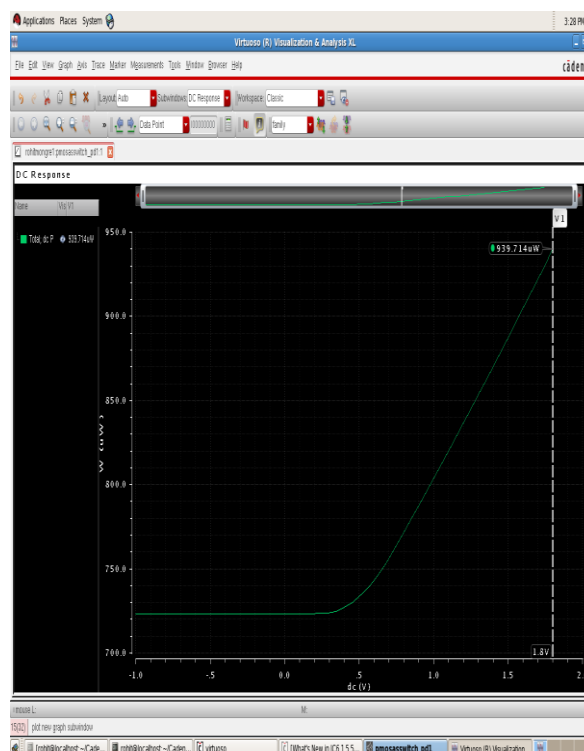Fig:15 Transient Analysis of dynamic comparator with positive feedback using PMOS as switch

IV. SIMULATION RESULTS AND DISCUSSION

Finally simulations of the comparator designs is done in cadence virtuoso with 0.18μm UMC Technology . Simulation results are presented including power dissipation, speed and delay. In these designs we have used single power supply i.e. 1.8 V. Through simulation we have obtained parameters of the comparator like power dissipation, clock frequency, time delay . In this work four comparator designs i.e preamplifier based fig:5, dynamic comparator, dynamic comparator with positive feedback, dynamic comparator with positive feedback using PMOS as switch has been simulated to obtain the low power and high speed parameters as it is required for robustness of the A/D converters. Final simulation results of the comparators are shown in Table1 and Table2.

TABLE 1:SIMULATED POWER DISSIPATION OF COMPARATORS.

TYPES OF COMPARATOR	TECHNOLOGY USED	POWER SUPPLY	POWER DISSIPATION
DESIGN I	0.18μm	1.8v	108.0318μW
DESIGN II	0.18μm	1.8v	605.57mW
DESIGN III	0.18μm	1.8v	939.879 μW
DESIGN IV	0.18μm	1.8v	939.714 μW

TABLE 2: SIMULATED RESULTS OF COMPARATOR.

TYPE OF COMPARATOR	Vir ps/ns	Vif Ps/ns	Vor Ps/ns	Vof Ps/ns	DELAY	SPEED= 1/DELAY Ghz
DESIGN I	2.7777ns	27.222ns	3.6864ns	28.7801ns	1.2333 ns	0.8108
DESIGN II	2.7777ns	27.222 ns	4.0752 ns	29.8079 ns	1.9416 ns	0.515
DESIGN III	55.5555 ps	20.1444 ns	164.496 ps	22.0799 ns	1.0222 ns	0.9782
DESIGN IV	55.5555 ps	20.1444 ns	156.277 ps	22.2280 ns	1.1171 ns	0.8951

V. CONCLUSION

In this paper simulation have been done in cadence virtuoso with 0.18µm UMC Technology. Finally simulation results of the comparators are shown in Table1 and Table2. As per the requirement of high speed and low power dissipation, DesignI i.e preamplifier based comparator having power dissipation of 108.0318µW , speed 0.8108 Ghz and delay of 1.2333ns confirms the expected circuit performance.

VI. ACKNOLEGEMENT

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